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<b>PRE-APPEAL BRIEF REQUEST FOR REVIEW</b>		Docket Number (Optional) <b>AZMT 002P1</b>	
I hereby certify that this correspondence is being transmitted by facsimile under 37 C.F.R. §1.8 to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450. Facsimile No: (571) 273-8300. on <u>April 13, 2006</u> Signature <u>Kathleen Faughnan</u> Typed or printed name <u>Kathleen Faughnan</u>		Application Number <b>10/730,758</b>	Filed <b>12/8/03</b>
		First Named Inventor <b>Lee, David</b>	
		Art Unit <b>2814</b>	Examiner <b>Ha, Nathan W.</b>
Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.  This request is being filed with a notice of appeal.  The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.			
I am the <input type="checkbox"/> applicant/inventor. <input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96) <input type="checkbox"/> attorney or agent of record. Registration number _____ <input checked="" type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 <u>51,359</u>		<u>AL QIL</u> Signature <b>Alan Taboada</b> Typed or printed name <b>(732) 935-7100</b> Telephone number <u>4/13/06</u> Date	
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.			
<input type="checkbox"/> *Total of _____ forms are submitted			

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PAGE 6/11 \* RCVD AT 4/13/2006 5:03:04 PM [Eastern Daylight Time] \* SVR:USPTO-EFXXF-2/14 \* DNIS:2738300 \* CSID:7329357122 \* DURATION (mm-ss):04-10

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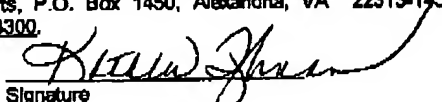
**IN THE UNITED STATES  
PATENT AND TRADEMARK OFFICE****RECEIVED  
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Applicant: **David Lee**  
Serial No.: **10/730,758**  
Examiner: **Ha, Nathan W.**  
Confirmation No.: **3464**

Case: **AZMT-002-P1**  
Filed: **December 8, 2003**  
Group Art Unit: **2814**

Title: **METHOD AND APPARATUS FOR PACKAGING ELECTRONIC  
COMPONENTS**

Mail Stop AF  
Commissioner for Patents  
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Alexandria, VA 22313-1450

<b>CERTIFICATE OF FACSIMILE TRANSMISSION UNDER 37 C.F.R. 51.8</b>	
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<u>4-13-06</u> Date	 Signature

S I R:

**REMARKS ACCOMPANYING PRE-APPEAL BRIEF REQUEST FOR REVIEW**

In response to the Final Office Action dated October 13, 2005, having a statutory period set to expire on April 14, 2006, please consider this Pre-Appeal Brief Request for Review (*Request*), submitted together with a Notice of Appeal, to review the clear error of the Examiner with respect to the pending claims.

Specifically, Appellant requests review of the clear error of the Examiner in improperly combining references to assert a rejection under 35 USC §103(a), namely, the rejection of claims 1-7 and 9-11 as being unpatentable over U.S. Patent No. 6,268,236 (hereinafter *Miyawaki*) in view of U.S. Patent No. 4,897,508 (hereinafter *Mahulikar*).

Appellant's invention, as recited in claim 1, molds sidewalls onto a substrate to form a plurality of cavities surrounding a component-mounting surface, wherein a component, such as an electronic component, may be mounted on the component-mounting surface in each cavity. Appellant's invention further includes curing a plurality of lids to the sidewalls, thereby creating component packages, and separating the component packages to form individually packaged components. Further, Appellant's invention includes a vent hole in each lid to facilitate the removal of reaction by-products from each cavity generated during the curing process.

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The Examiner contends that *Miyawaki* discloses a method of packaging at least one component, comprising: providing a lid; molding sidewalls, for example, onto a substrate to form a plurality of cavities surrounding a component-mounting surface; mounting a component on the component-mounting surface in each capacity, applying a curable adhesive to a top surface of the sidewalls; placing the lid upon the surface of the sidewall; curing said adhesive; and separating the component package into a plurality of individual component packages. (*Final Office Action*, ¶2). The Examiner cites *Mahulikar* as teaching an analogous package including a substrate, a cavity, and a component in the cavity, with an adhesive layer to attach a lid to the substrate, with the lid comprising a vent hole for releasing reaction by-products generated during the cure cycle. The Examiner concludes that a combination of the teachings of *Miyawaki* and *Mahulikar* teaches the Appellant's invention. (*Id.*) Appellant respectfully disagrees.

*Miyawaki* clearly teaches, at col. 2, l. 66 – col. 3, l. 1, that the base package substrate 1 is created by bonding together a lower first substrate 1A and an upper second substrate 1B having a grid-like pattern of rectangular through-holes. Both the lower first substrate and upper second substrate are formed prior to being adhered to one another. For example, at col. 3, ll. 8-12, the reference teaches, "(t)hrough holes or penetrating holes are formed in the second (upper) substrate 1B in order to produce hollow cavities." The substrates 1A and 1B are then "stacked into the single base substrate 1, thereby constituting a substrate having a plurality of cavities." Clearly, the method of stacking and bonding together preformed substrates 1A and 1B, as taught by *Miyawaki*, does not teach nor suggest molding sidewalls onto a substrate to form a plurality of cavities, as recited in Appellant's claim 1.

With respect to *Mahulikar*, by inspection of any of FIGS. 1, 3, or 4 (and the corresponding written descriptions), it is easily determined that *Mahulikar* teaches fastening a leadframe 16 to a base 12 with a first sealant 28 and subsequently fastening a cover component 14 to the leadframe 16 with a second sealant 26 (see, at least, *Mahulikar*, col. 3, ll. 21-24; col. 4, ll. 8-12). Thus, as applicable here, the reference distinctly teaches nothing more than sealants applied for bonding the base,

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leadframe, and cover component. As such, it is respectfully submitted that one skilled in the art would not be led by the combination of cited references to create a molded package in the manner claimed.

Accordingly, neither *Miyawaki* nor *Mahulikar*, together or singly, teach the step of "molding sidewalls onto a substrate to form a plurality of cavities surrounding a component-mounting surface," as recited in claim 1. Consequently, a *prima facie* case of obviousness has not been established because *Miyawaki* and *Mahulikar*, either alone or in combination, fail to teach or suggest the limitations recited in the claims.

In the Advisory Action dated January 18, 2006, the Examiner responded to Appellant's arguments by asserting that "several methods of forming a substrate are discussed [in *Miyawaki*]. For instance, *Miyawaki* discusses that the hollow package, or cavity, can be formed by using conventional molding method, and this method is well known and commonly used." The Examiner asserts that this disclosure teaches or suggests the step of molding sidewalls onto a substrate. (*Advisory Action*, p. 3). The Appellant disagrees.

The Examiner is erroneously interpreting the teachings of *Miyawaki*. Specifically, *Miyawaki* clearly differentiates between the use of a hollow cavity and a molded cavity for encapsulating a component. (*See, at least, Miyawaki*, col. 1, ll. 16-25). In the Background of the *Miyawaki* patent, *Miyawaki* states that although a "commonly-used mold package" may be used to encapsulate components, there are drawbacks associated with this method. (*Id.*) *Miyawaki* describes one such molding method where "a substance, such as epoxy resin having a large dielectric constant comes into close contact with a semiconductor chip...thereby introducing parasitic capacitance and deteriorating the characteristics of the semiconductor package." (*Id.*) Throughout the disclosure, *Miyawaki* emphasizes that his embodiments overcome the drawbacks associated with this type of molding process while achieving similar benefits as those attained through this type of molding process. (*See, at least, Miyawaki*, col. 4, ll. 51-60, and col. 8, ll. 4-7). However, at no place in *Miyawaki*, either at the location cited by the Examiner or elsewhere, is a molding process disclosed that teaches or suggests the step of molding sidewalls onto a substrate to form a plurality of cavities.

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as recited in claim 1. In fact, the invention as claimed by Appellant overcomes the same drawbacks of the conventional molding process as outlined *Miyawaki*. For example, in the Background of the Related Art section of the present application, the Appellant describes the same, or similar, conventional molding process as discussed in *Miyawaki*. (10/730,758, ¶[0004].)

Thus, both *Miyawaki* and the Appellant discuss the drawbacks of conventional molding processes and have developed methods to overcome those drawbacks. Accordingly, rather than “render[ing] [obvious] the process of creating cavities by [a] molding process,” (as asserted by the Examiner in the *Final Office Action*, p. 5, ¶[4], in fact, *Miyawaki* actually teaches away from using a molding process. Therefore, *Miyawaki* fails to teach or suggest molding sidewalls onto a substrate to form a plurality of cavities surrounding a component-mounting surface, as recited in claim 1.

In the Advisory Action dated January 18, 2006, the Examiner further asserts that “[f]or example, fig. 2C shows a few substrates that have sidewalls molded onto, so a better sealing may be established.” (*Advisory Action*, p. 3)(emphasis added). The Appellant disagrees.

Contrary to the Examiner's assertion, Figure 2C of *Miyawaki* does not show substrates that have sidewalls molded onto, but, in fact, shows multiple cavities created by bonding a lower first substrate 1A and a pre-formed upper second substrate 1B to create a base substrate 1, followed by the sealing of a cap member 2 by adhesive 3. (*Miyawaki*, col. 2, l. 66 – col. 3, l. 1; col. 3, ll. 19-24.) As discussed above, *Miyawaki* discloses a method of forming an semiconductor device package that overcomes the problems associated by conventional molding processes. Thus, the embodiments cited by the Examiner (and all other embodiments taught or suggested by *Miyawaki*) fail to disclose a “substrate having sidewalls molded onto,” but rather show the bonded upper and lower preformed substrates as taught by *Miyawaki* to overcome the drawbacks of the molding process. As such, *Miyawaki* fails to teach or suggest molding sidewalls onto a substrate to form a plurality of cavities surrounding a component-mounting surface, as recited in claim 1.

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Accordingly, as *Mahulikar* fails to teach or suggest a modification of *Miyawaki* that would result in the step of molding sidewalls onto a substrate to form a plurality of cavities surrounding a component-mounting surface, as recited in claim 1, a *prima facie* case of obviousness has not been established because the combination of *Miyawaki* and *Mahulikar* fails to the limitations recited in the claims.

Thus, independent claim 1 and claims 2-7 and 9-11, depending therefrom, are patentable over *Miyawaki* in view of *Mahulikar*. Accordingly, Appellant requests that the rejection be withdrawn and the claims allowed.

In the Final Office Action dated October 13, 2005, the Examiner rejected claim 8, dependent from claim 1, under 35 U.S.C. §103(a) as being unpatentable over both *Miyawaki* and *Mahulikar* in further view of U.S. Patent No. 5,776,799 issued to Song (hereinafter "*Song*"). Along with the above discussion, Appellant reasserts the arguments made on page 5 of the Response filed August 2, 2005 and page 5 of the Response filed December 12, 2005 that dependent claim 8 is patentable over *Miyawaki* in view of *Mahulikar* and further in view of *Song*. Accordingly, Appellant requests that this rejection be withdrawn and that the claim be allowed.

Thus, Appellant submits that all claims now pending are in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issuance are earnestly solicited. If, however, the Examiner believes that there are any unresolved issues in the application, it is requested that the Examiner telephone Mr. Alan Taboada at (732) 935-7100 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,



4/13/06

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